

1/20

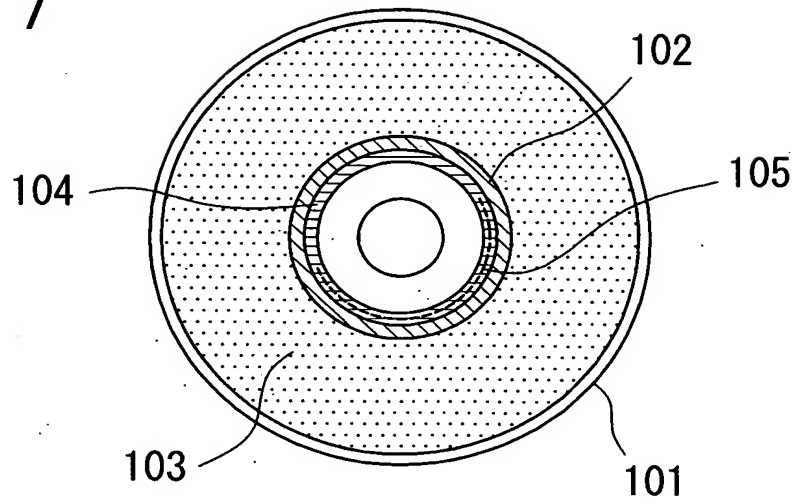
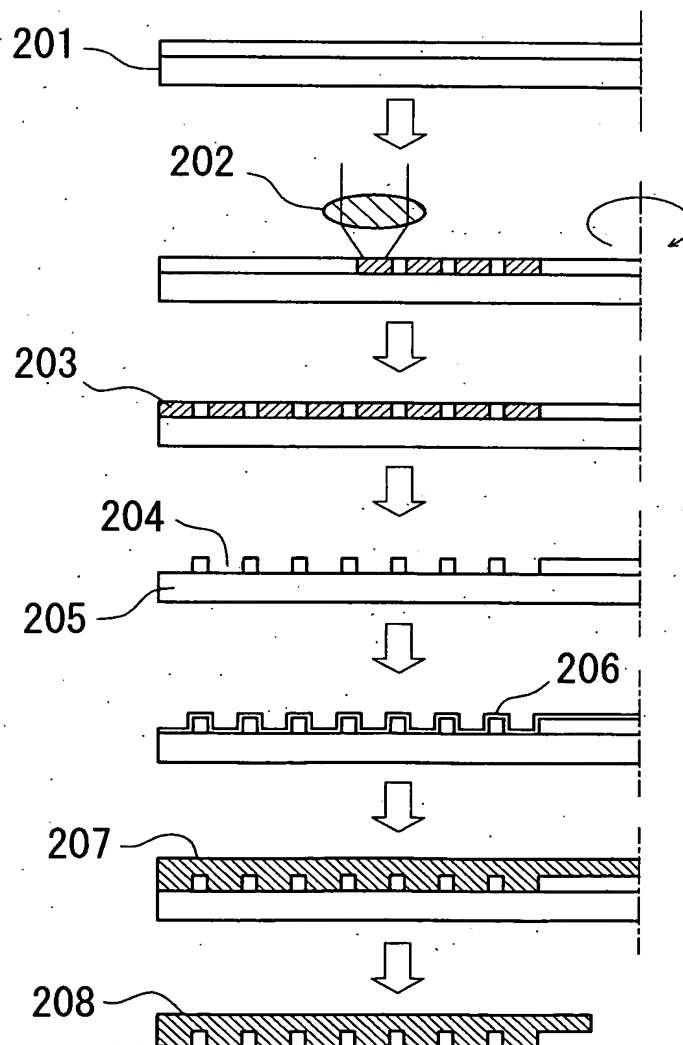
Fig. 1*Fig. 2*

Fig. 3

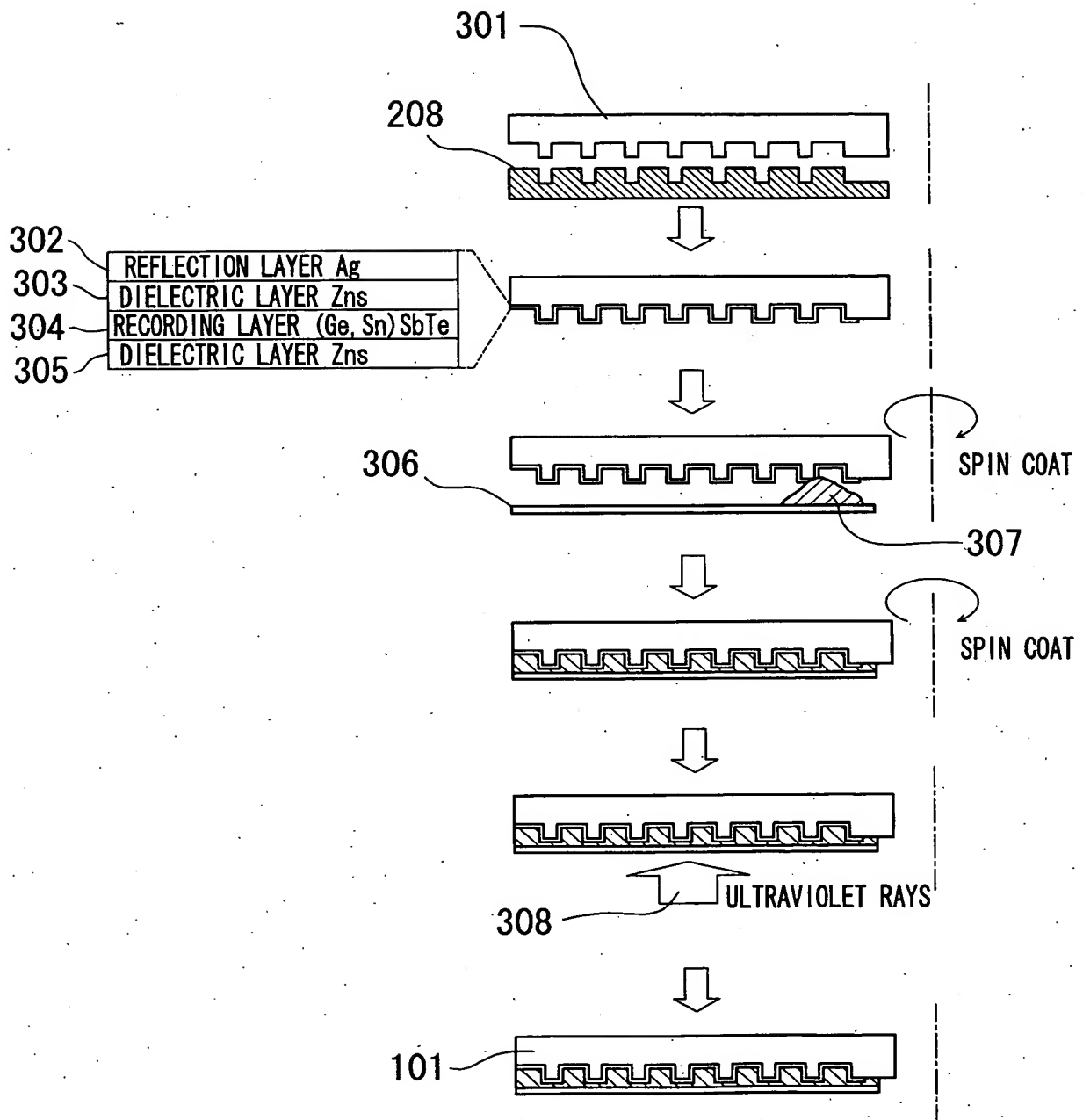


Fig. 4

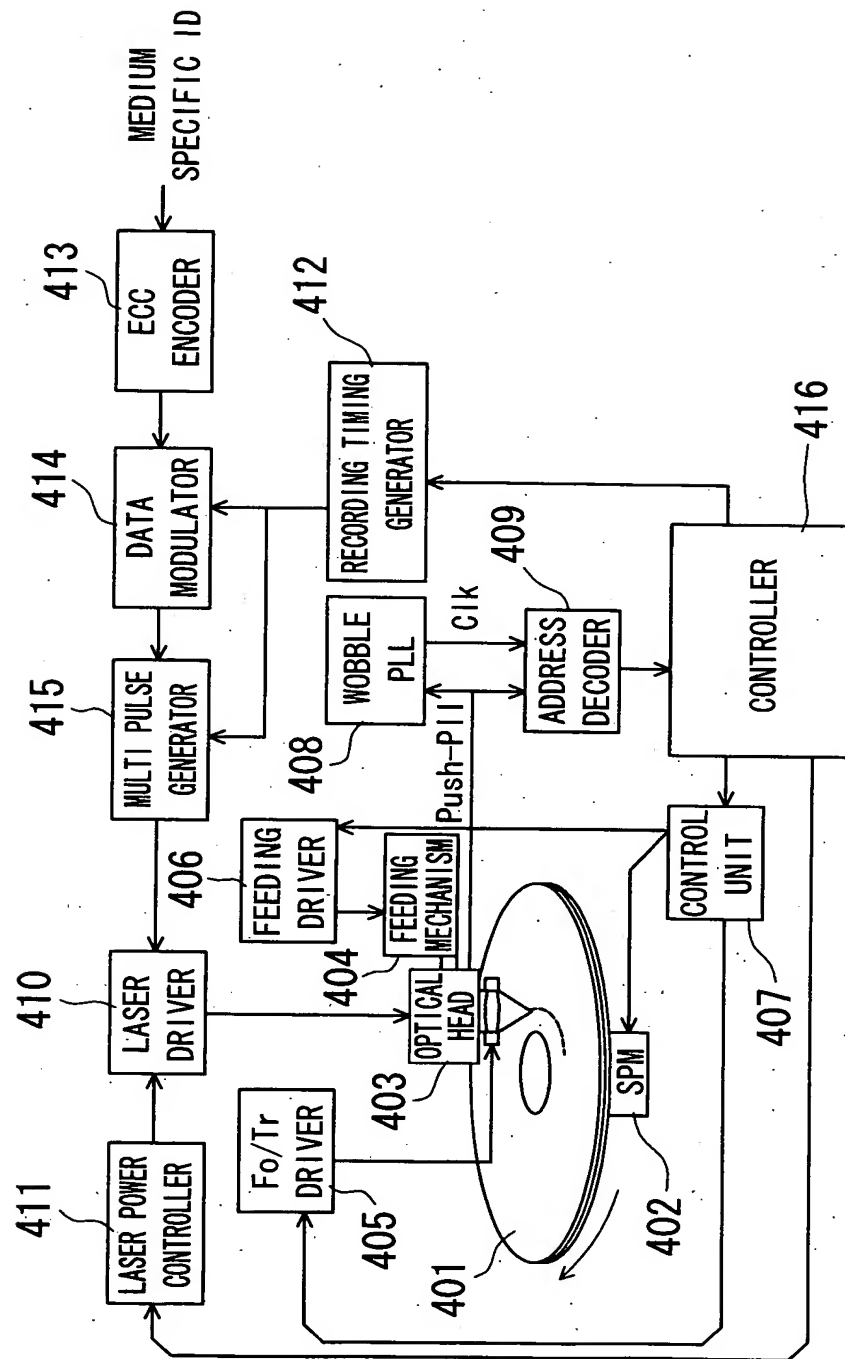


Fig. 5A

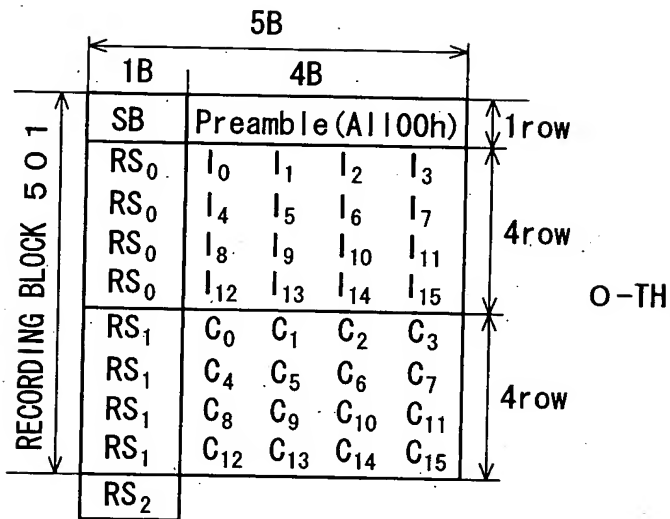


Fig. 5B

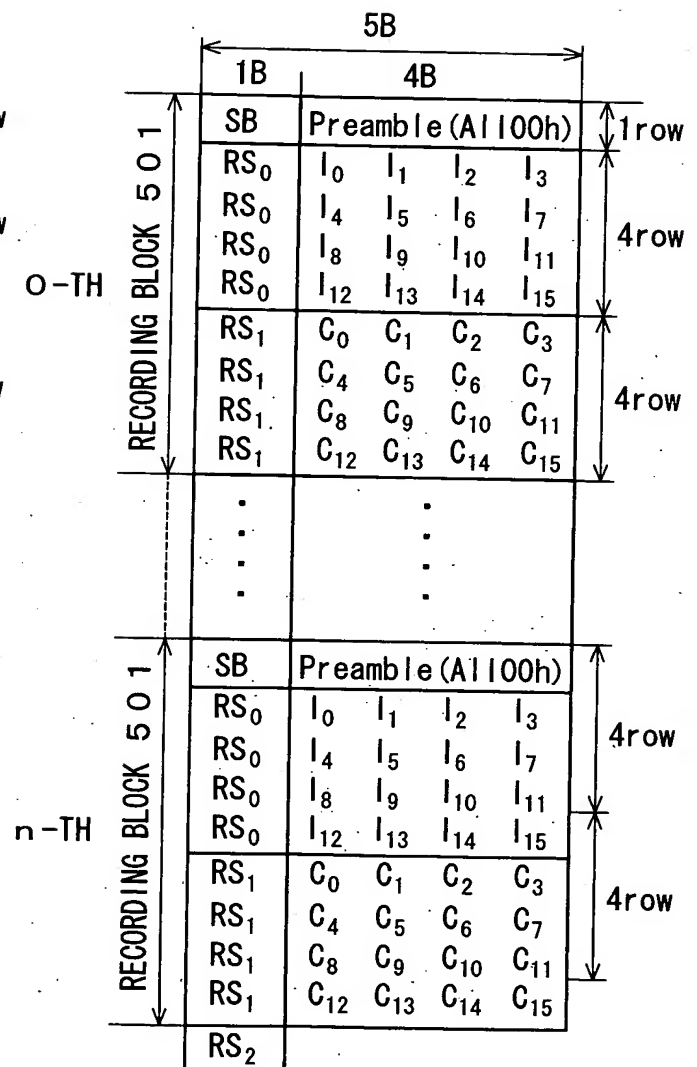


Fig. 6

SYNC MARK	BIT PATTERN
SB	1001010000100001
RS ₀	1001010000101001
RS ₁	1001010000100011
RS ₂	1001010000110001

Fig. 7

DATA BIT	MODULATED DATA BITS
0	10
1	01

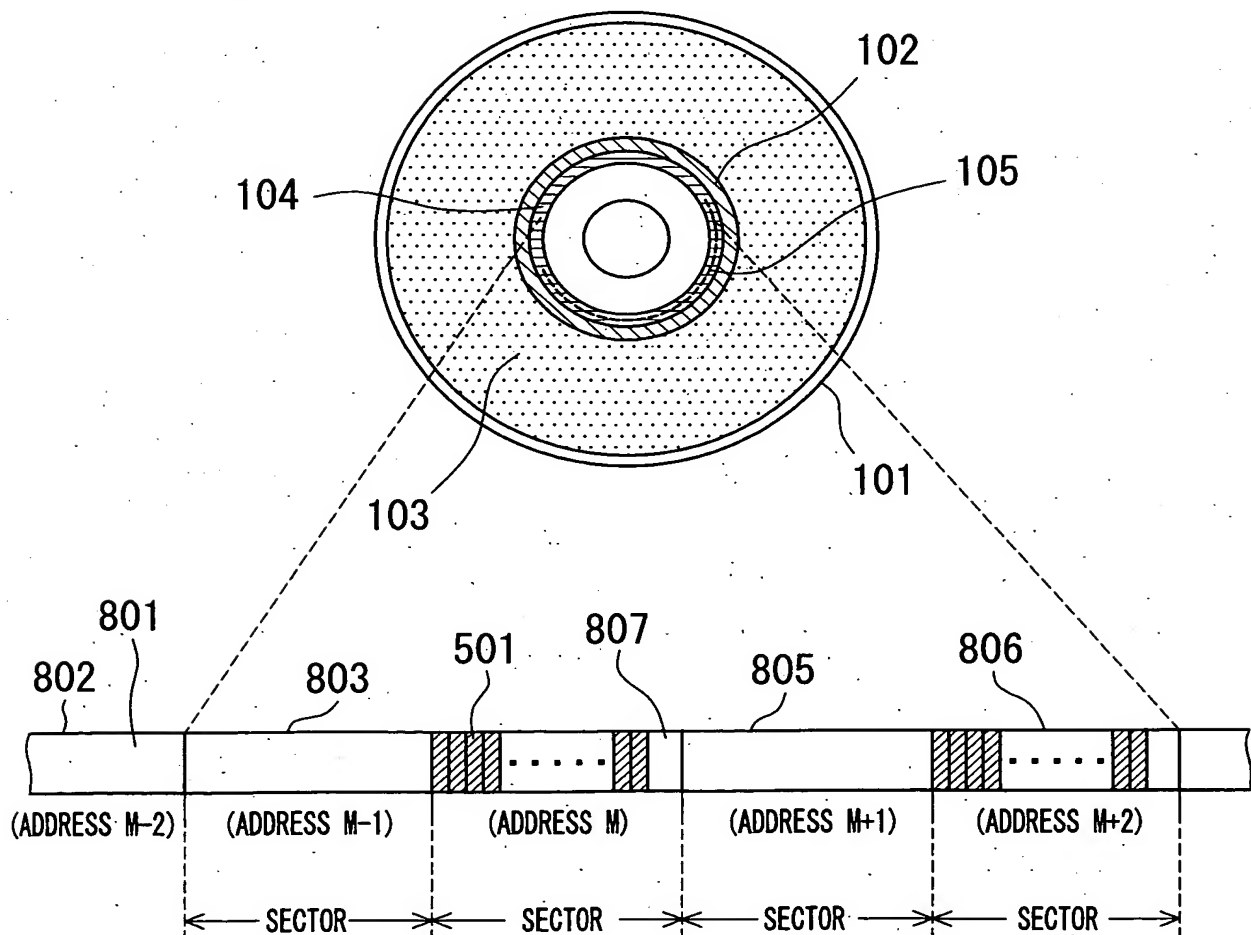
Fig. 8

Fig. 9A

Fig. 9B

Fig. 9C

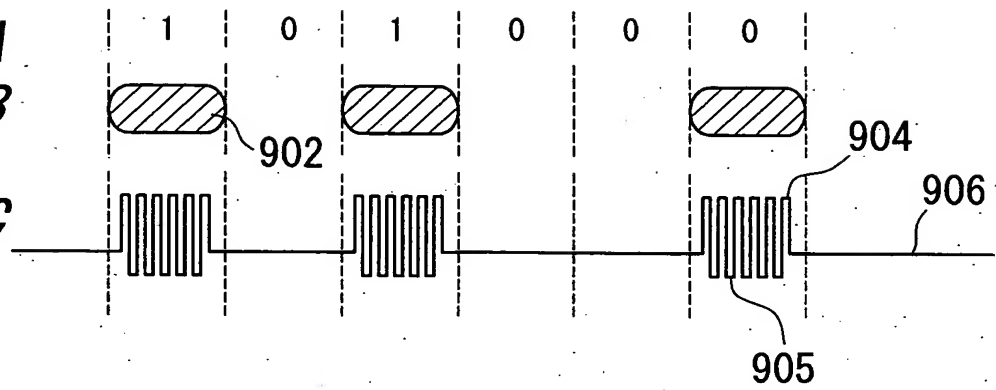


Fig. 10A

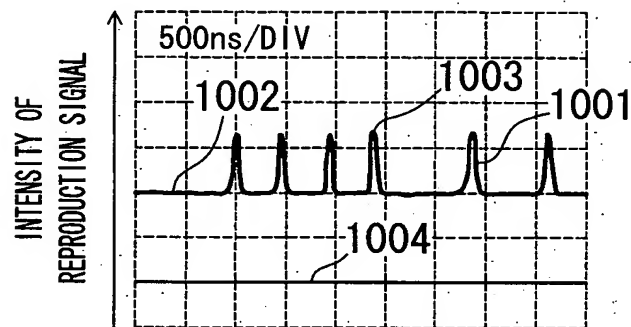


Fig. 10B

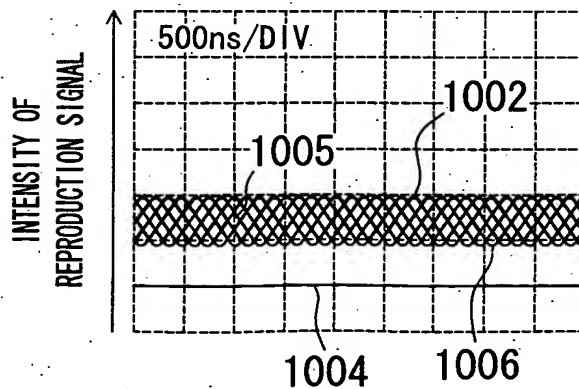


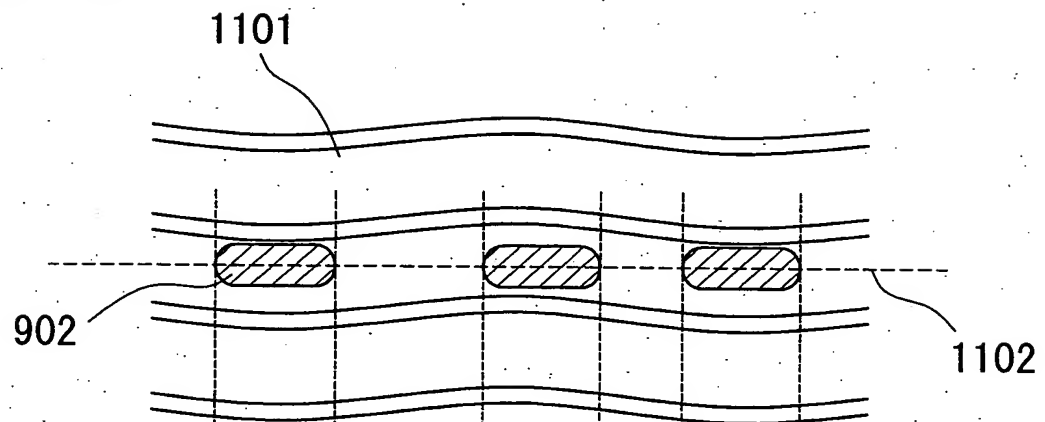
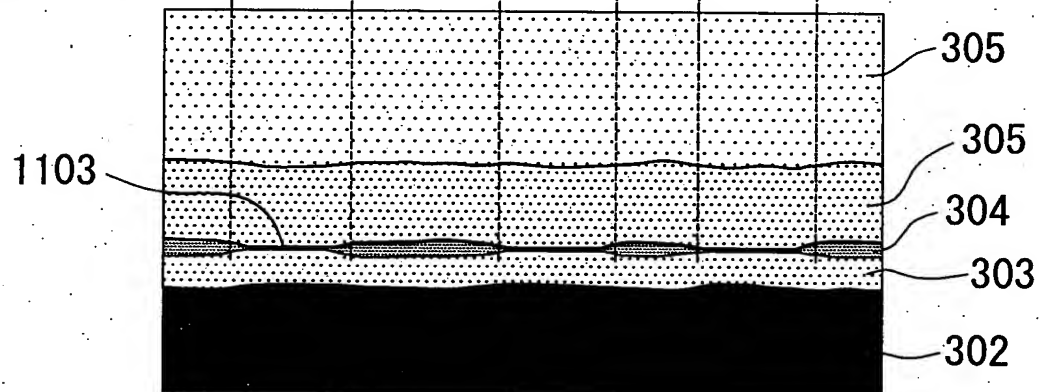
Fig. 11A*Fig. 11B*

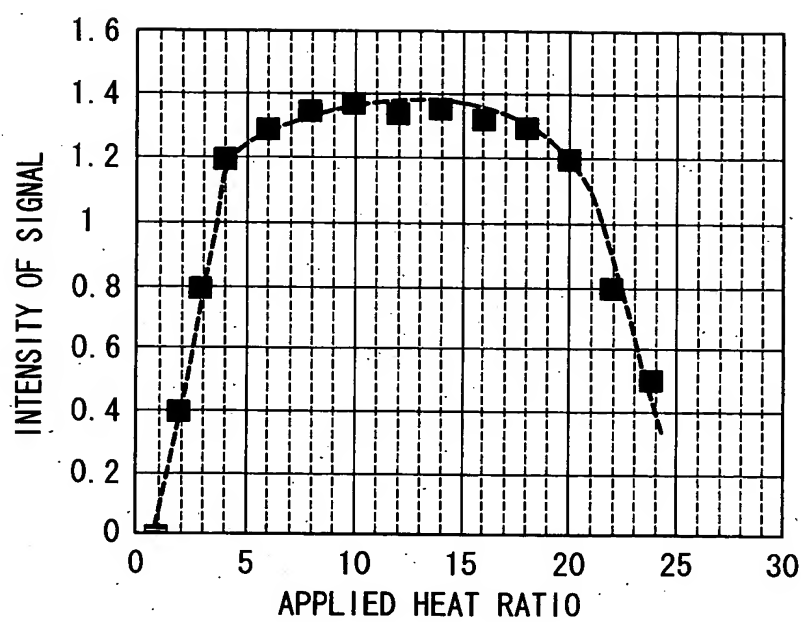
Fig. 12

Fig. 13

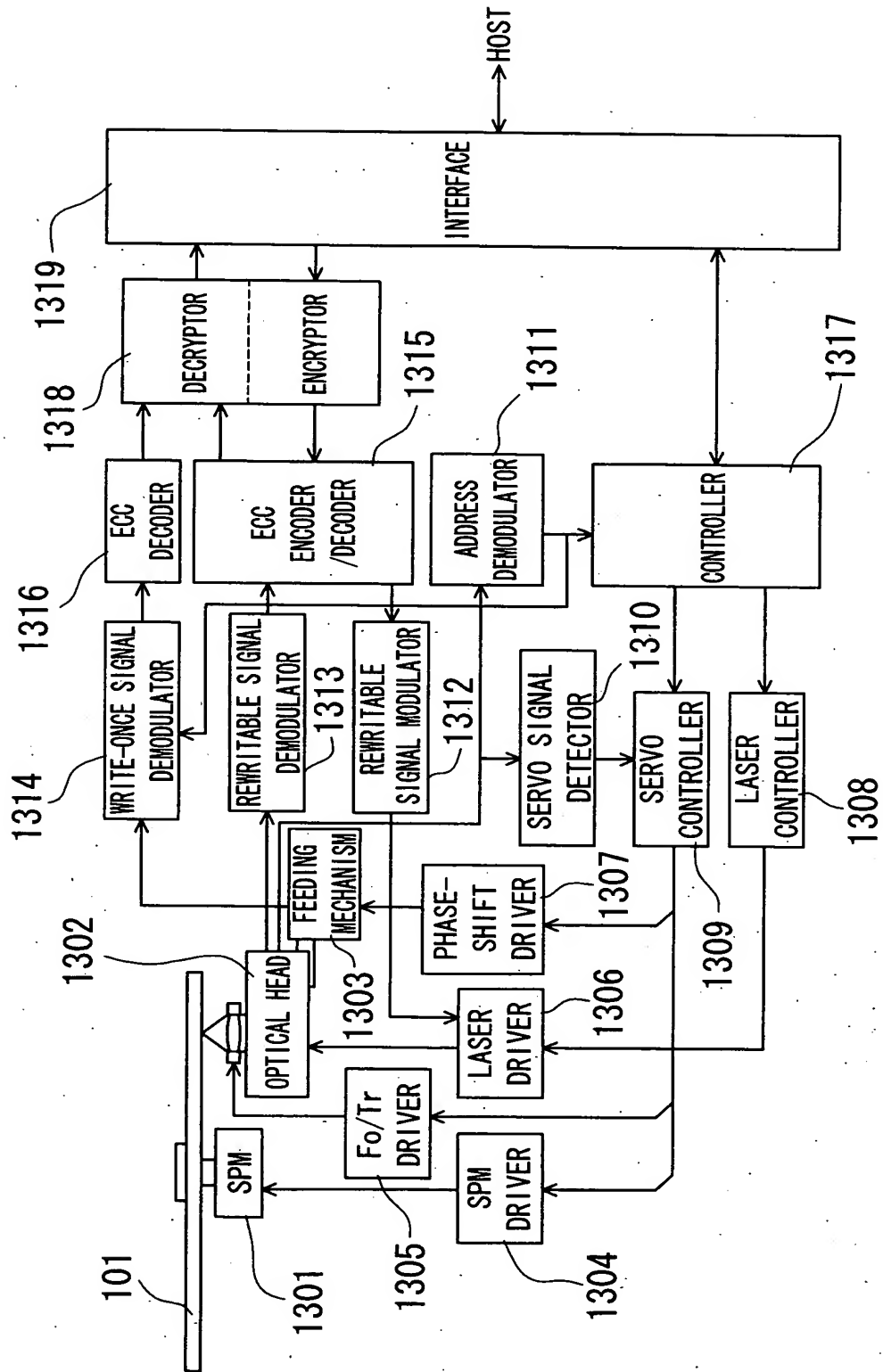


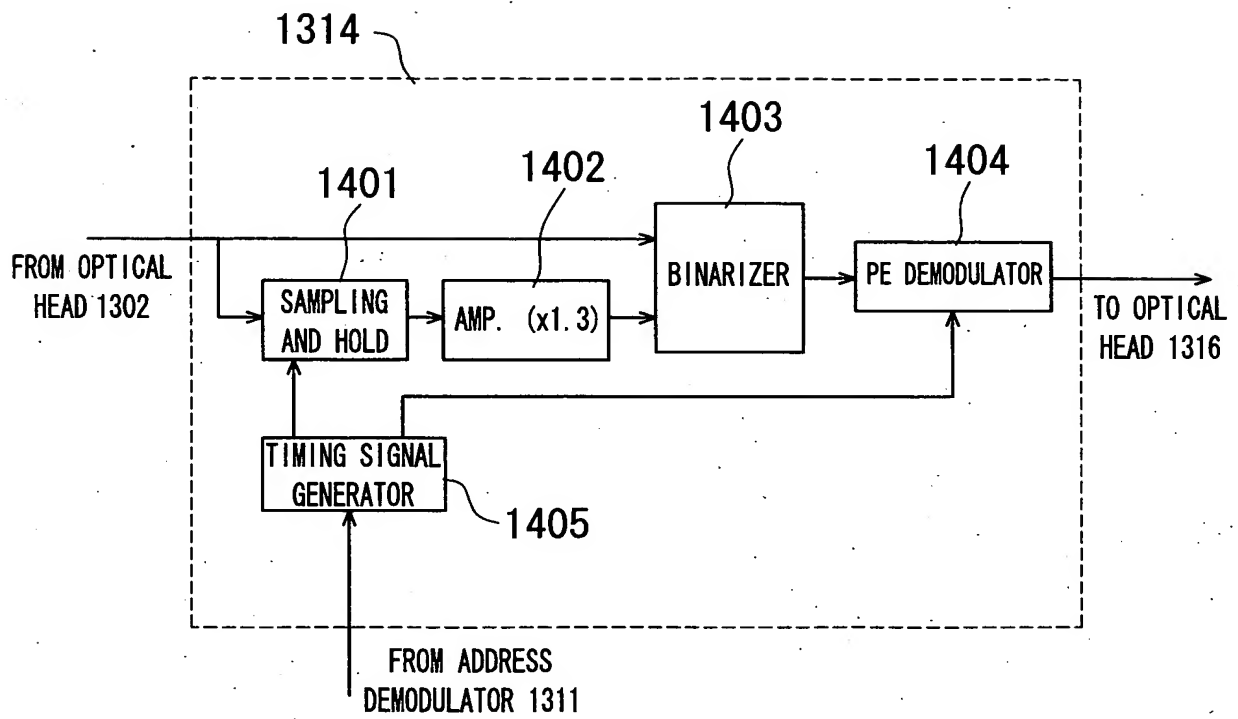
Fig. 14

Fig. 15

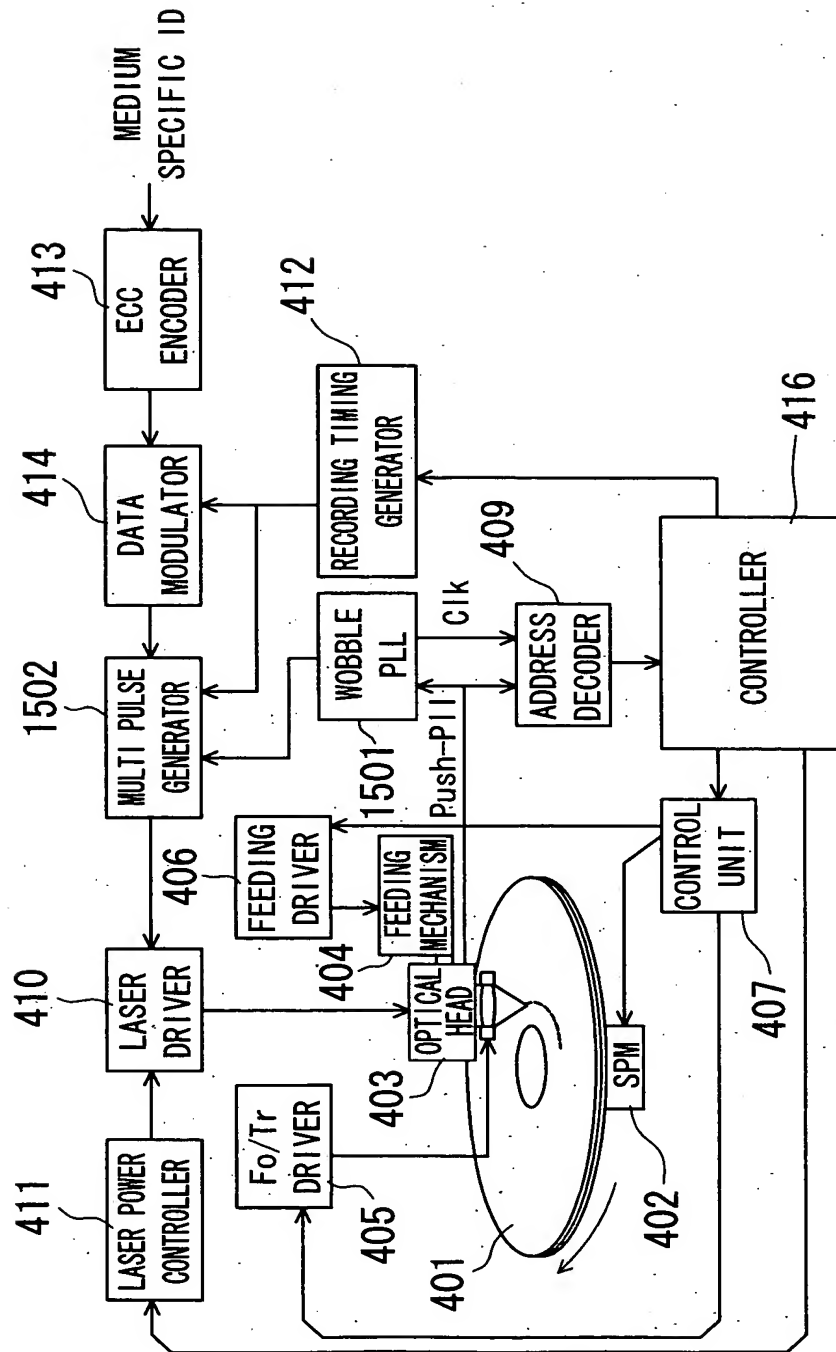


Fig. 16A

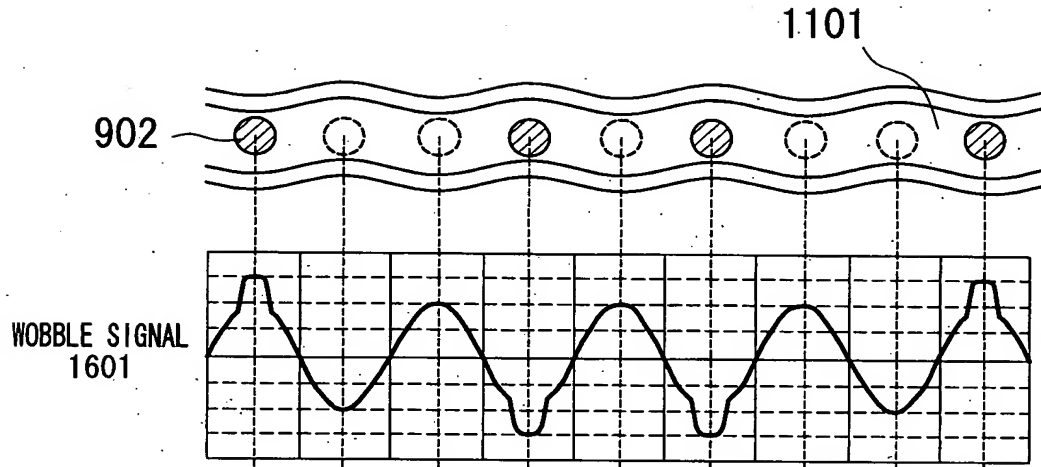


Fig. 16B

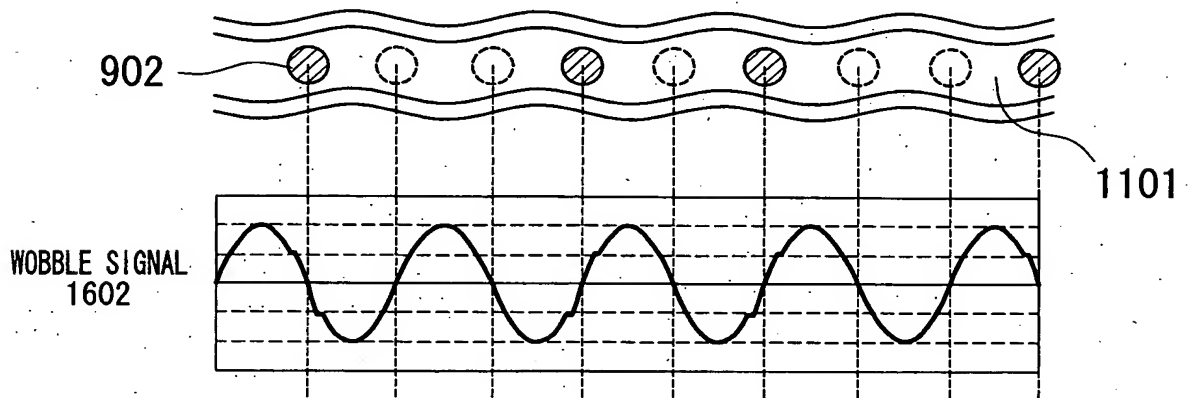


Fig. 18

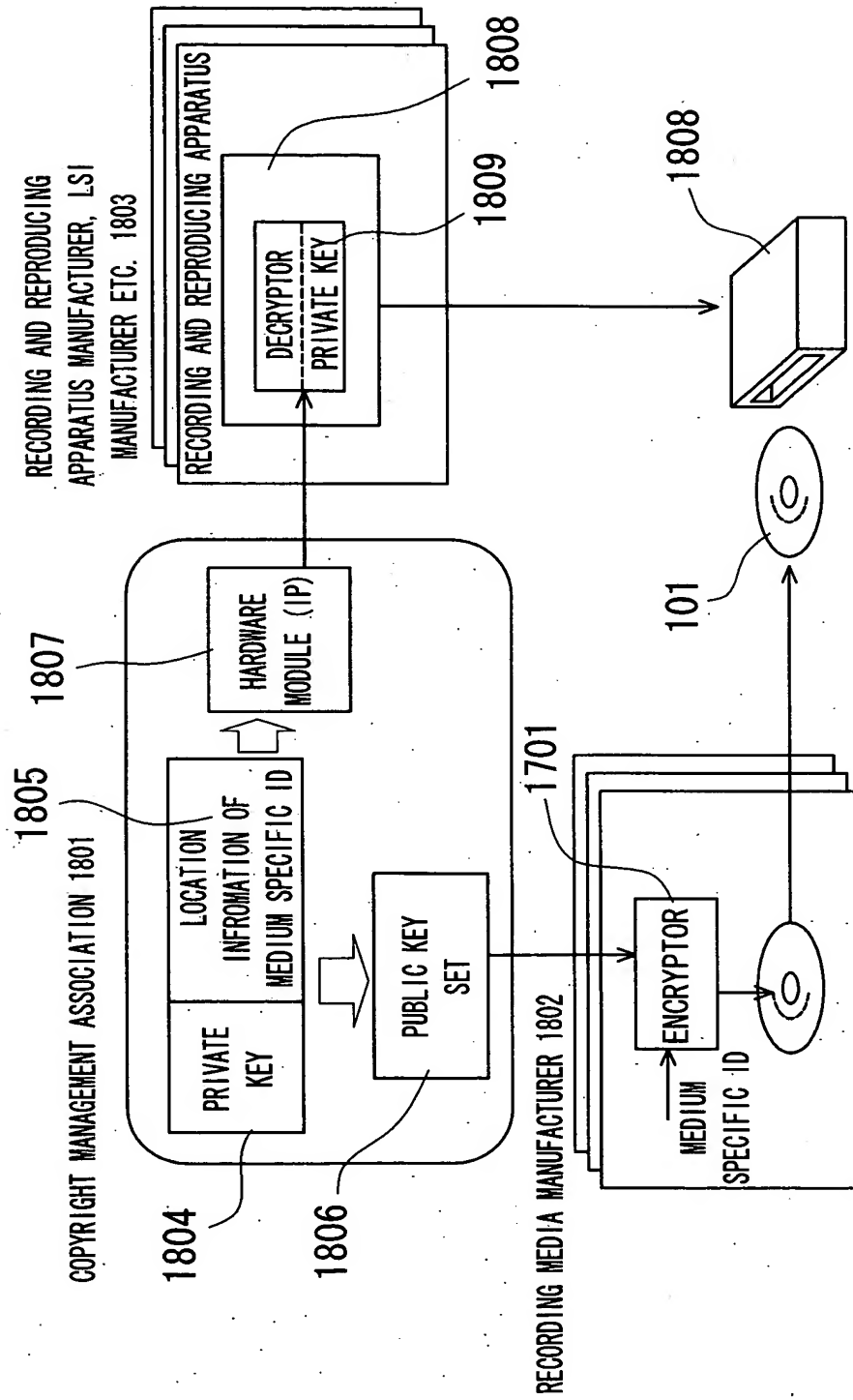


Fig. 19

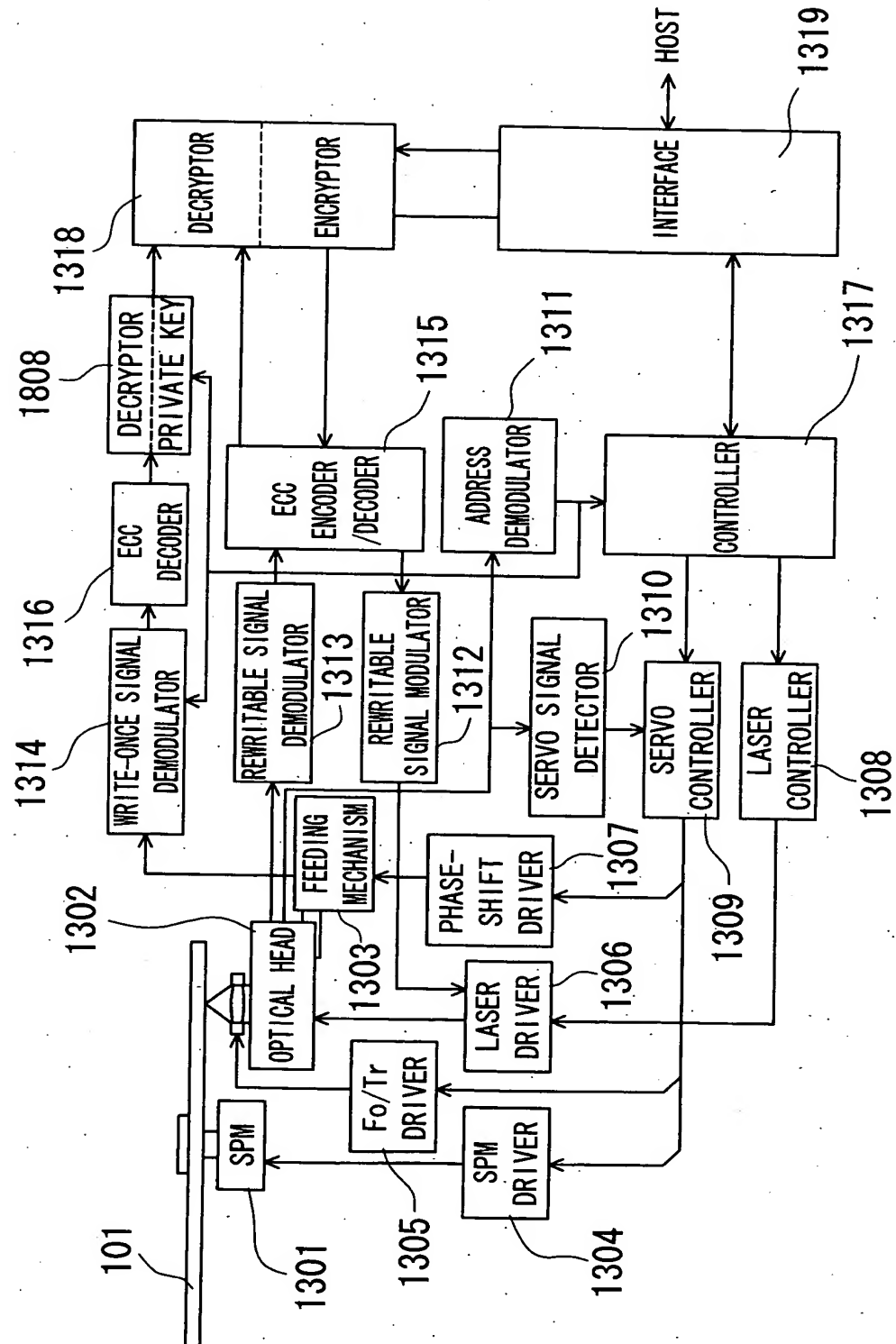


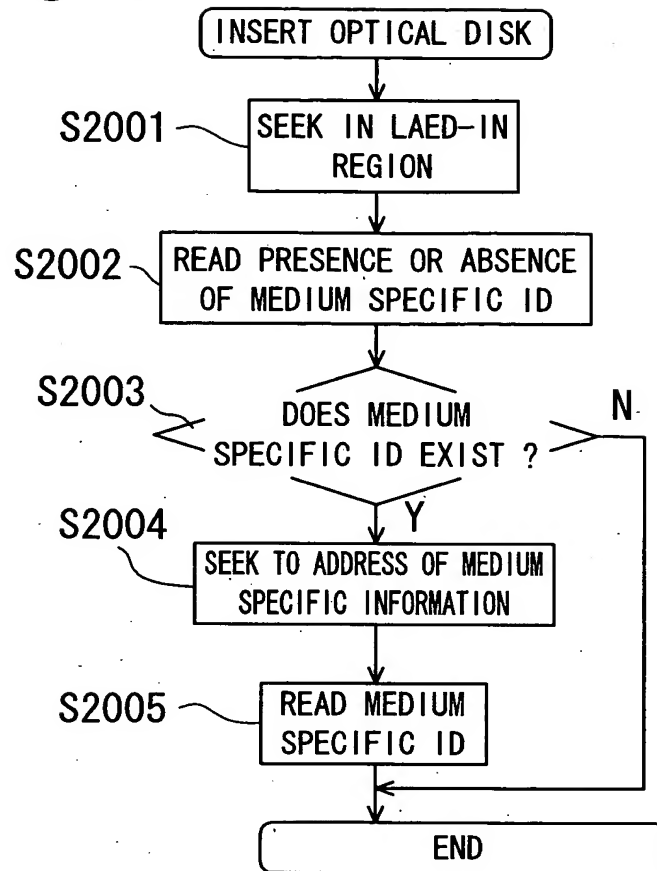
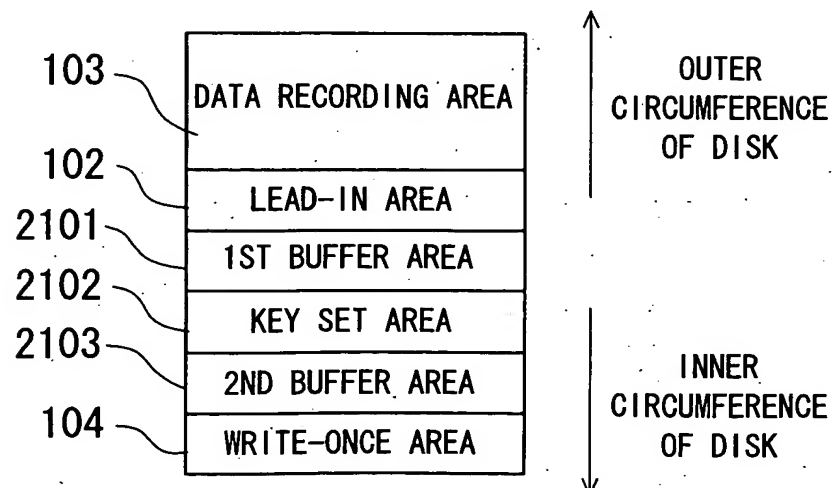
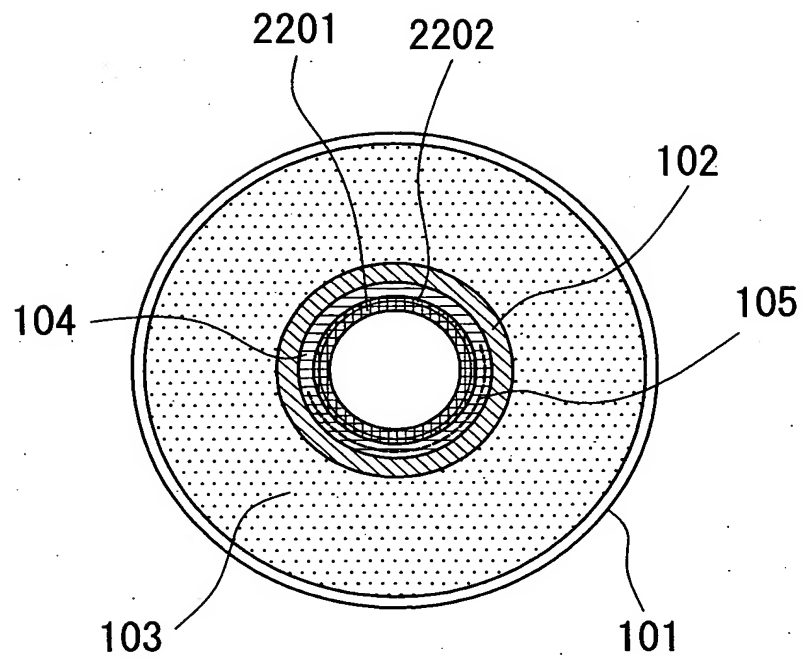
Fig. 20*Fig. 21*

Fig. 22

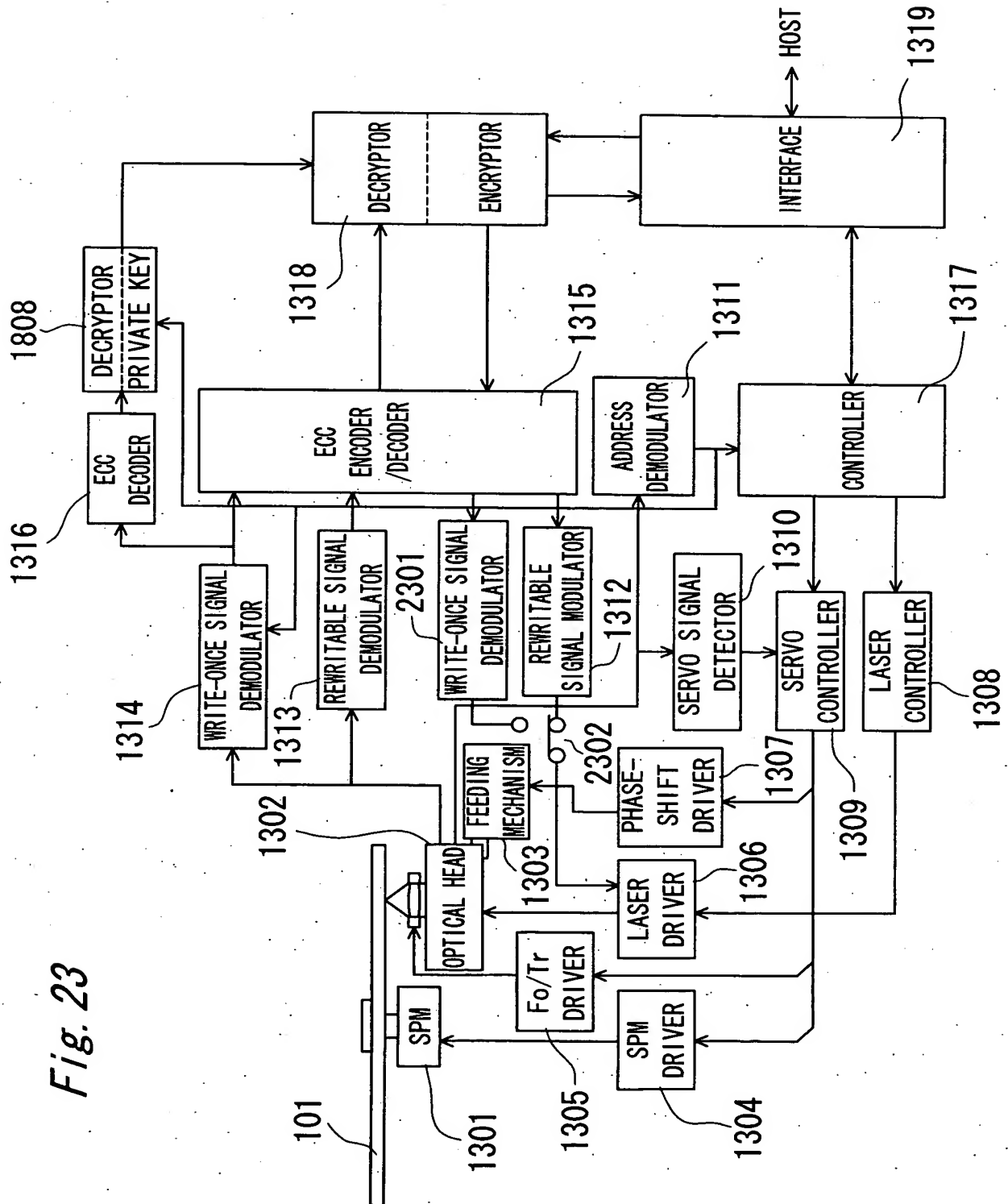


Fig. 23

Fig. 24

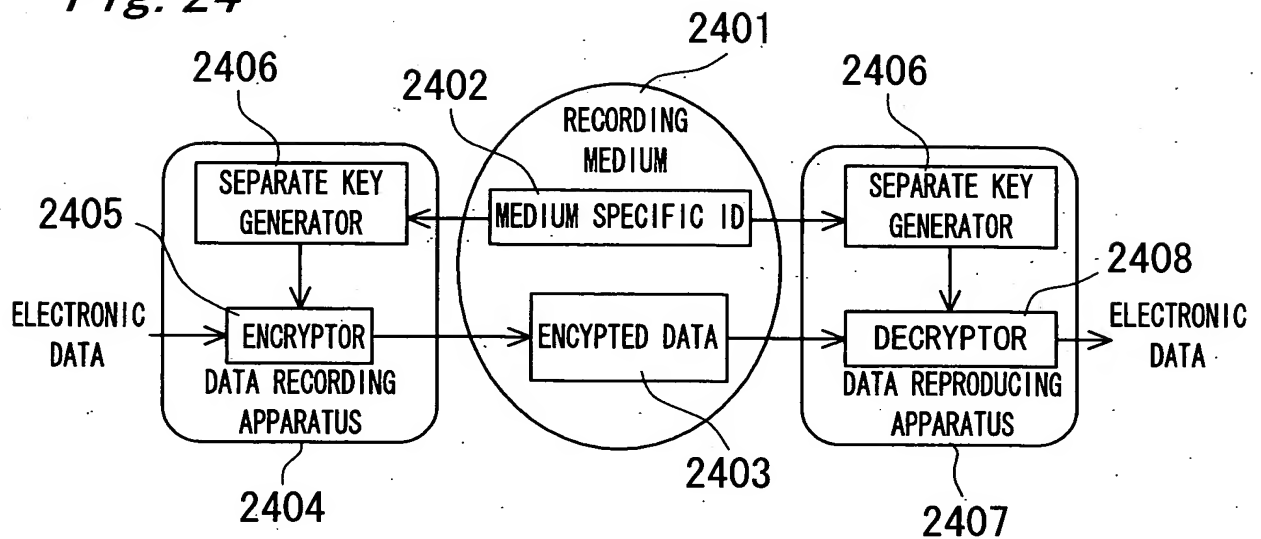


Fig. 25

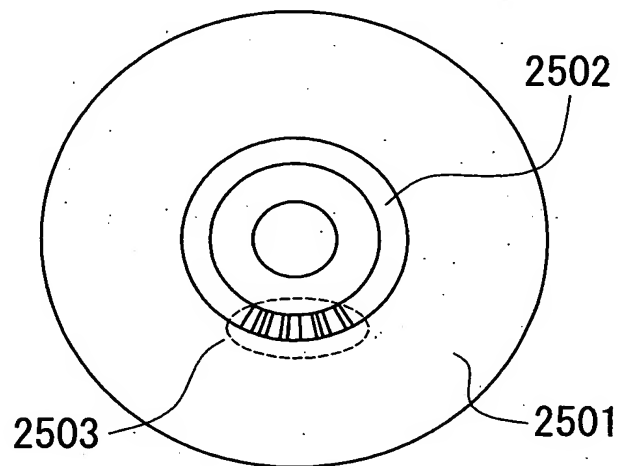


Fig. 26

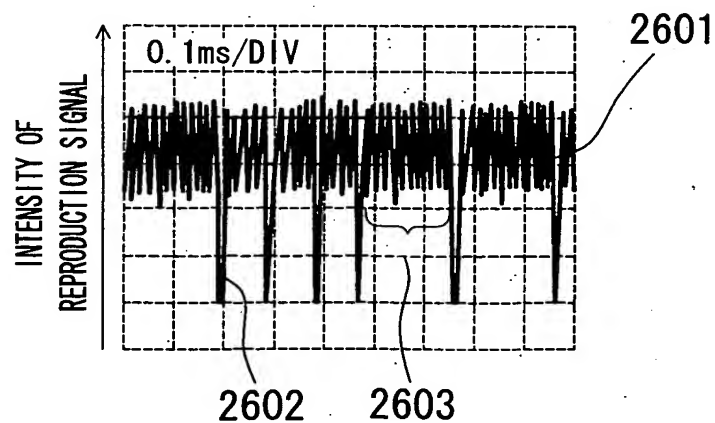


Fig. 27